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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,665	11/03/2001	Eric R. Alling	50781	7668

21874 7590 10/05/2004

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EXAMINER	
MUTSCHLER, BRIAN L	

ART UNIT	PAPER NUMBER
1753	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,665	ALLING ET AL.	
	Examiner	Art Unit	
	Brian L. Mutschler	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Comments

1. The objection to claim 1 has been overcome by Applicant's amendment.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meltzer et al. (U.S. Pat. No. 6,547,946) in view of Akram et al. (U.S. Pat. No. 5,893,966), with evidence of physical properties provided by CRC Handbook of Chemistry and Physics ("Thermal and Physical Properties of Pure Metals", 3rd Electronic Edition).

Regarding claim 1, Meltzer et al. disclose a method for depositing multiple metal layers on a printed wiring board by single bath deposition, wherein a copper layer and a nickel layer are plated from a single bath containing a copper metal source and a nickel metal source (fig. 1; col. 5, lines 8-52). Copper is plated using a low reduction potential and nickel is plated using a high reduction potential, and the reduction potentials differ by more than 0.2 V (fig. 3; col. 5, lines 8-28). The nickel layer "contains a percentage of

copper", which means the nickel layer is actually an alloy of nickel and copper (col. 5, lines 35-37). Additionally, the plating composition comprises additional metals such as manganese, chromium, zinc, iron, cobalt, cadmium, tin, lead, arsenic, antimony, bismuth, gold, and silver (col. 7, lines 56-67). The nickel layer is an insulator according to both definitions described explained above. First, as seen in the table "Thermal and Physical Properties of Pure Metals", in the CRC Handbook of Chemistry and Physics, the resistivity of nickel is over 400% greater than the resistivity of copper. Second, the nickel layer acts as an "etch resist" layer, thus acting to isolate or insulate the copper layer from an etching solution (col. 5, lines 29-37). The copper layer forms copper circuitry (col. 5, lines 29-37).

Regarding claim 2, the copper layer is formed as a homogenous layer (col. 5, lines 29-31).

Regarding claim 3, the nickel layer "contains a percentage of copper", which means the nickel layer is actually an alloy of nickel and copper (col. 5, lines 35-37).

Regarding claim 7, Meltzer et al. disclose that the method for fabricating the layered printed wiring board was "adapted from layered electroforming techniques used to build up copper-nickel composite materials of high tensile strength [and t]hese materials typically had many alternating, very thin layers of each metal" (col. 5, lines 55-59). Additionally, Meltzer et al. teach that that the deposition of copper and nickel layers may be repeated more than 100 times, which would result in alternating layers of copper and nickel (col. 10, lines 60-61).

The method of Meltzer et al. differs from the instant invention because Meltzer et al. do not disclose that the substrate is a semiconductor microchip wafer substrate, as recited in claim 1.

Regarding claim 1, Akram et al. teach, "Semiconductor wafers, substrates and printed circuit boards (collectively hereinafter 'semiconductor substrates') are often coated with various metals" (col. 1, lines 16-20). Furthermore, Akram et al. teach, "Techniques for coating semiconductor substrates include electrodeposition...[and e]lectrodeposition has become a commonly used technology" (col. 1, lines 21-24).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the substrate used in the method of Meltzer et al. to use a semiconductor microchip wafer substrate because Akram et al. teach that semiconductor substrates are commonly coated using electrodeposition techniques and that equivalent semiconductor substrates include semiconductor wafers, substrates and printed circuit boards.

Response to Arguments

4. Applicant's arguments filed September 30, 2004, have been fully considered but they are not persuasive.

5. Regarding the rejection of the claims, Applicant argues, "Contrary to the apparent position in the Office Action, persons skilled in the art recognize that plating copper on a microelectronic wafer is quite difficult, and poses unique issues relative to plating

copper on other substrates such as printed circuit board" (see page 5 of Applicant's response). In support of this argument, Applicant has cited excerpts from U.S. Pat. No. 6,290,833; U.S. Pat. No. 6,297,154; and U.S. Pat. No. 6,171,960.

6. This argument is not persuasive because Akram et al. clearly teach that electrodeposition is commonly used for both semiconductor wafers and printed circuit boards (see US '966 at col. 1, lines 15-24). Therefore, it would have been obvious to one of ordinary skill in the art that both printed circuit boards and semiconductor wafers can be electroplated. Therefore, it would have been obvious to one skilled in the art that a single bath plating method known for electroplating printed circuit boards could similarly be used to electroplate semiconductor wafers.

7. The passages cited by Applicant are not persuasive. Regarding US '833, Applicant draws attention to the passage regarding the difficulties of depositing copper metallization due to the need for barrier layer materials (see page 5 of Applicant's response). This is not persuasive because Akram et al. acknowledge that "the electrodeposition process is relatively complex," but like the reference cited by the Applicant, Akram et al. also disclose how these complexities are dealt with (see US '966 at col. 1, lines 47+). Since the prior art teaches how these difficulties are overcome, Applicant's argument is not persuasive because it is not clear what difficulties Applicant had to overcome. Meltzer et al. clearly teach a method having all of the limitations recited in the instant claims except for the substrate that is electroplated. Since Akram et al. teach that semiconductor wafers and printed circuit boards can both be

electroplated, there do not appear to be any difficulties remaining that are not within the skill of the ordinary artisan.

8. Applicant also cites US '154 to show that the "problem with faulty fill-up increases with increasing aspect ratio" (see page 6 of Applicant's response). It is unclear how this passage relates to the instant claims because the claims do not recite the presence of voids. Therefore, there is no difficulty presented by an increasing aspect ratio. Furthermore, increased aspects ratios similarly affect both printed circuit board substrates and semiconductor wafer substrates.

9. Applicant relies on US '960 to suggest that "[m]any problems, however, are encountered in fabricating circuit interconnects with copper" (see page 6 of Applicant's response). It is unclear how this passage relates to the instant claims. These difficulties are present in any copper plating method and are not specific to either the claimed method or the method taught by Meltzer et al. It is unclear how these difficulties preclude one skilled in the art from using the method of Meltzer et al. to plate a semiconductor wafer as taught by Akram et al.

10. Applicant further states, "Akram et al. also does not identify any specific metals being deposited by the reported method" (see page 6 of Applicant's response). This statement is not persuasive because the reference of Akram et al. is relied upon to show that electrodeposition methods can be used for both printed circuit boards and semiconductor wafers.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (571) 272-1341. The examiner can normally be reached on Monday-Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BLM
September 30, 2004